CBCS/B.Sc./Hons./Programme/4th Sem./CMSHGEC04T/CMSGCOR04T/2021

WEST BENGAL STATE UNIVERSITY

B.Sc. Honours/Programme 4th Semester Examination, 2021

CMSHGEC04T/CMSGCOR04T-COMPUTER SCIENCE (GE4/DSC4)

COMPUTER SYSTEM ARCHITECTURE

Time Allotted: 2 Hours

The figures in the margin indicate full marks. Candidates should answer in their own words and adhere to the word limit as practicable. All symbols are of usual significance.

Question No. 1 is compulsory. In addition answer any four from the rest

- 1. Answer any *four* questions from the following:
 - (a) Differentiate between combinational circuit and sequential circuit.
 - (b) How to represent a binary floating point number?
 - (c) What is meant by instruction?
 - (d) What is propagation delay of a circuit?
 - (e) Why Gray Code is called a unit-distance code?
 - (f) What do you mean by addressing mode?
 - (g) Draw a NAND gate using only NOR gates.
 - (h) Differentiate between a latch and a flip-flop.
- 2. Define signed and unsigned binary numbers. What are the advantages of using 2's 3+3+2 complement representation over 1's complement representation of binary numbers? Perform the following:

$$(1011)_2 + (1100111)_2 = (?)_{16}$$

3. Simplify the following expression into SOP using K map 4+4 $F(w, x, y, z) = \sum m(0, 1, 2, 4, 5, 12, 13, 14) + \text{don't care conditions } \sum d(6, 8, 9)$. Realize it using only NAND gates.

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- 4. (a) What is the role of Program Counter?
 - (b) Realize a full adder circuit using half adders.





 $2 \times 4 = 8$

Full Marks: 40

4 + 4

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5. (a) Implement a 8-to-1 MUX using two 4-to-1 MUX.	4+4
(b) What is magnitude comparator? Write the truth table and draw the logic circuit of a single-bit magnitude comparator.	
6. (a) What is JK flip-flop? Draw a JK flip-flop using only NAND gates.	4+2+2
(b) What is a Race Around condition in JK flip-flop?	
(c) Why JK flip-flop is preferred over SR flip-flop?	
7. (a) Define the terms Instruction Cycle, Fetch Cycle, Execute Cycle.	6+2
(b) What is a System Bus?	
8. Write short notes on (any <i>two</i>):	4×2 = 8
(a) Cache Memory	
(b) Memory Hierarchy	

- (c) Synchronous Counter vs. Asynchronous Counter
- (d) Direct addressing mode vs. Indirect addressing mode.
 - **N.B.**: Students have to complete submission of their Answer Scripts through E-mail / Whatsapp to their own respective colleges on the same day / date of examination within 1 hour after end of exam. University / College authorities will not be held responsible for wrong submission (at in proper address). Students are strongly advised not to submit multiple copies of the same answer script.

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